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Code No.: 21115 O3

VASAVI COLLEGE OF ENGINEERING (Autonomous), HYDERABAD
B.E. II Year (C.S.E.) I-Semester Supplementary Examinations, May/June-2017

Computer Architecture

Time: 3 hours

Max. Marks: 70

Note: Answer ALL questions in Part-A and any FIVE from Part-B

Part-A (10 X 2=20 Marks)

- Convert the following decimal numbers to the bases indicated.
i) 7562 to octal ii) 1734 to hexadecimal
- What is bus structure? Give its elements.
- Name logic micro-operations with example.
- What is an overflow? How it is detected?
- Give the advantages of Micro programmed control unit.
- List the sequence of Zero - address instructions for the following example
 $X = (A+B) * (C+D)$
- Differentiate memory mapped I/O and isolated I/O.
- What is UART? Give its significance.
- An address space is specified by 24 bits and the corresponding memory space by 16 bits.
a) How many words are there in the address space?
b) How many words are there in the memory space?
- Define CPU performance.

Part-B (5 × 10 = 50 Marks)

- a) Draw various computer components and explain them. [5]
b) Compute subtraction of the following numbers using 2's complement representation. [5]
(i) 11010 - 1101 (ii) 100 - 110000
- a) Explain shift microoperations with examples. [5]
b) The content of PC in the basic computer is 3AF (all numbers are in hexa decimal). The content of AC is 7EC3. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. [5]
i) What is the instruction that will be fetched and executed next?
ii) Show the binary operation that will be performed in the AC when the instruction is executed.
iii) Give the contents of registers PC, AR, DR, AC, and IR in hexadecimal and the values of E, I, and the sequence counter SC in binary at the end of the instruction cycle.
- a) Illustrate Booth's multiplication algorithm with example. [6]
b) What is a 64- word stack? Explain the operations implemented with 64- word stack along with sequence of microoperations. [4]

- 14. a) Describe an asynchronous data transfer using strobe control with the help of timing diagram. [5]
- b) A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slowed down because of the DMA transfer? [5]
- 15. a) What is the use of cache memory? And Describe direct and associative mapping techniques of cache memory. [8]
- b) What are the factors used for measuring CPU performance? [2]
- 16. a) Explain different types of signed integer representation with examples. [4]
- b) Describe Common Bus system with neat diagram. [6]
- 17. Write short notes on any two of the following:
 - a) Address sequencing in microprogrammed control unit [5]
 - b) Daisy chain priority management [5]
 - c) Auxiliary Memory [5]
